



Amendments of the Claims

The following listing of claims, if entered, will replace all prior versions, and listings, of claims in the above-identified patent application:

Listing of Claims

1. (currently amended) A phase-locked loop circuit for use in a programmable logic device, said phase-locked loop circuit having an input terminal for receiving an input signal having a reference frequency and an output
5 terminal for outputting an output frequency phase-locked to said reference frequency, and comprising:
an oscillator for producing said output frequency; and
a feedback path feeding said oscillator, said
10 feedback path accepting as inputs said reference frequency and said output frequency, and causing said oscillator to drive said output frequency to a phase-frequency lock with said reference frequency, said feedback path comprising at least one component connected therein; wherein:
15 ~~at least one~~ or more of said at least one component is programmably connectable to another portion of said programmable logic device for operation of said another portion of said programmable logic device with said ~~at least one~~ or more of said at least one component.
2. (currently amended) The phase-locked loop circuit of claim 1 wherein, when said phase-locked loop circuit is not in use in said programmable logic device, said
5 ~~at least one~~ or more of said at least one component is available for use by said another portion of said programmable logic device.
3. (currently amended) The phase-locked loop circuit of claim 1 wherein, when said phase-locked loop circuit is in use in said programmable logic device, said another portion of said programmable logic device is

5 available to be substituted in said phase-locked loop circuit
for said ~~at least one~~ or more of said at least one component.

4. (previously presented) The phase-locked loop
circuit of claim 1 wherein said at least one component
comprises:

a phase-frequency detector having as inputs
5 said reference frequency and said output frequency, said
phase-frequency detector outputting a comparison signal
indicating a relationship between said reference frequency
and said output frequency;

an analog front end circuit having said
10 comparison signal as an input and outputting an analog
voltage signal indicative of said comparison;

an analog-to-digital converter having said
analog voltage signal as an input and outputting a digitized
voltage signal;

15 a digital signal processor having said
digitized voltage signal as an input and outputting a digital
control signal; and

a digital-to-analog converter having said
digital control signal as an input and outputting an analog
20 control signal that is input to said oscillator.

5. (original) The phase-locked loop circuit of
claim 4 wherein said analog-to-digital converter has at least
one of:

a second input from a first said another
5 portion of said programmable logic device; and

a second output to a second said another
portion of said programmable logic device.

6. (original) The phase-locked loop circuit of
claim 5 wherein said first said another portion is a pin of
said programmable logic device.

7. (original) The phase-locked loop circuit of
claim 5 wherein said first said another portion is in core
logic of said programmable logic device.

8. (original) The phase-locked loop circuit of claim 5 wherein said second said another portion is a pin of said programmable logic device.

9. (original) The phase-locked loop circuit of claim 5 wherein said second said another portion is in core logic of said programmable logic device.

10. (previously presented) The phase-locked loop circuit of claim 4 wherein said digital signal processor has at least one of:

a second input programmably connectable to a
5 first said another portion of said programmable logic device;
and

a second output programmably connectable to a
second said another portion of said programmable logic
device.

11. (original) The phase-locked loop circuit of claim 10 wherein said first said another portion is a pin of said programmable logic device.

12. (original) The phase-locked loop circuit of claim 10 wherein said first said another portion is in core logic of said programmable logic device.

13. (original) The phase-locked loop circuit of claim 10 wherein said second said another portion is a pin of said programmable logic device.

14. (original) The phase-locked loop circuit of claim 10 wherein said second said another portion is in core logic of said programmable logic device.

15. (currently amended) The phase-locked loop circuit of claim 4 wherein said digital-to-analog converter has at least one of:

a second input programmably connectable to a
5 first said another portion of said programmable logic device;
and

a second output programmably connectable to a
second said another portion of said programmable logic
device.

16. (original) The phase-locked loop circuit of
claim 15 wherein said first said another portion is a pin of
said programmable logic device.

17. (original) The phase-locked loop circuit of
claim 15 wherein said first said another portion is in core
logic of said programmable logic device.

18. (original) The phase-locked loop circuit of
claim 15 wherein said second said another portion is a pin of
said programmable logic device.

19. (original) The phase-locked loop circuit of
claim 15 wherein said second said another portion is in core
logic of said programmable logic device.

20. (original) The phase-locked loop circuit of
claim 4 wherein said analog front end circuit comprises a
charge pump.

21. (previously presented) The phase-locked loop
circuit of claim 1 wherein said at least one component
comprises:

a phase-frequency detector having as inputs
5 said reference frequency and said output frequency, said
phase-frequency detector outputting digital comparison
signals indicating a relationship between said reference
frequency and said output frequency;

a digital counter circuit having said digital
10 comparison signals as inputs and outputting digital count
signals indicative of said comparison;

a digital signal processor having said digital count signals as inputs and outputting a digital control signal; and

15 a digital-to-analog converter having said digital control signal as an input and outputting an analog control signal that is input to said oscillator.

22. (previously presented) The phase-locked loop circuit of claim 21 wherein said digital signal processor has at least one of:

an additional input programmably connectable
5 to a first said another portion of said programmable logic device; and

a second output programmably connectable to a second said another portion of said programmable logic device.

23. (original) The phase-locked loop circuit of claim 22 wherein said first said another portion is a pin of said programmable logic device.

24. (original) The phase-locked loop circuit of claim 22 wherein said first said another portion is in core logic of said programmable logic device.

25. (original) The phase-locked loop circuit of claim 22 wherein said second said another portion is a pin of said programmable logic device.

26. (original) The phase-locked loop circuit of claim 22 wherein said second said another portion is in core logic of said programmable logic device.

27. (previously presented) The phase-locked loop circuit of claim 21 wherein said digital-to-analog converter has at least one of:

a second input programmably connectable to a
5 first said another portion of said programmable logic device;
and

a second output programmably connectable to a second said another portion of said programmable logic device.

28. (original) The phase-locked loop circuit of claim 27 wherein said first said another portion is a pin of said programmable logic device.

29. (original) The phase-locked loop circuit of claim 27 wherein said first said another portion is in core logic of said programmable logic device.

30. (original) The phase-locked loop circuit of claim 27 wherein said second said another portion is a pin of said programmable logic device.

31. (original) The phase-locked loop circuit of claim 27 wherein said second said another portion is in core logic of said programmable logic device.

32. (original) The phase-locked loop circuit of claim 1 wherein said oscillator is a voltage-controlled oscillator.

33. (original) The phase-locked loop circuit of claim 1 further comprising an output scaling counter downstream of said output terminal.

34. (original) The phase-locked loop circuit of claim 1 further comprising an input scaling counter upstream of said input terminal.

35. (original) The phase-locked loop circuit of claim 1 further comprising a feedback scaling counter between said output terminal and said feedback path.

36. (original) A programmable logic device comprising the phase-locked loop circuit of claim 1.

37. (original) A digital processing system comprising:

processing circuitry;
a memory coupled to said processing circuitry;
5 and
a programmable logic device as defined in
claim 36 coupled to the processing circuitry and the memory.

38. (original) A printed circuit board on which is
mounted a programmable logic device as defined in claim 36.

39. (original) The printed circuit board defined in
claim 38 further comprising:

memory circuitry mounted on the printed
circuit board and coupled to the programmable logic device.

40. (original) The printed circuit board defined in
claim 39 further comprising:

processing circuitry mounted on the printed
circuit board and coupled to the memory circuitry.

41. (original) An integrated circuit device
comprising the phase-locked loop circuit of claim 1.

42. (original) A digital processing system
comprising:

processing circuitry;
a memory coupled to said processing circuitry;

5 and
an integrated circuit device as defined in
claim 41 coupled to the processing circuitry and the memory.

43. (original) A printed circuit board on which is
mounted an integrated circuit device as defined in claim 41.

44. (original) The printed circuit board defined in
claim 43 further comprising:

memory circuitry mounted on the printed
circuit board and coupled to the integrated circuit device.

45. (original) The printed circuit board defined in
claim 44 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

46. (currently amended) A programmable logic device comprising:

at least one programmable logic region; and
a phase-locked loop circuit having an input
5 terminal for receiving an input signal having a reference frequency and an output terminal for outputting an output frequency phase-locked to said reference frequency, and comprising:

an oscillator for producing said output
10 frequency, and

a feedback path feeding said oscillator, said feedback path accepting as inputs said reference frequency and said output frequency, and causing said oscillator to drive said output frequency to a phase-frequency lock with
15 said reference frequency, said feedback path comprising at least one component connected therein, wherein:

~~at least one~~ or more of said at least one component is programmably connectable to said programmable logic region for operation of said programmable logic region
20 with said at least one of said at least one component.

47. (currently amended) The programmable logic device of claim 46 wherein, when said phase-locked loop circuit is not in use in said programmable logic device, said
~~at least one~~ or more of said at least one component is
5 available for use by said at least one programmable logic region.

48. (currently amended) The programmable logic device of claim 46 wherein, when said phase-locked loop circuit is in use in said programmable logic device, at least a portion of said at least one programmable logic region is
5 available to be substituted in said phase-locked loop circuit for said ~~at least one~~ or more of said at least one component.

49. (previously presented) The programmable logic device of claim 46 wherein said at least one component comprises:

- 5 a phase-frequency detector having as inputs said reference frequency and said output frequency, said phase-frequency detector outputting a comparison signal indicating a relationship between said reference frequency and said output frequency;
- 10 an analog front end circuit having said comparison signal as an input and outputting an analog voltage signal indicative of said comparison;
- an analog-to-digital converter having said analog voltage signal as an input and outputting a digitized voltage signal;
- 15 a digital signal processor having said digitized voltage signal as an input and outputting a digital control signal; and
- a digital-to-analog converter having said digital control signal as an input and outputting an analog control signal that is input to said oscillator.
- 20

50. (previously presented) The programmable logic device of claim 49 wherein said analog-to-digital converter has at least one of:

- 5 a second input programmably connectable to a first said another portion of said programmable logic device; and
- a second output programmably connectable to a second said another portion of said programmable logic device.

51. (original) The programmable logic device of claim 50 wherein said first said another portion is a pin of said programmable logic device.

52. (original) The programmable logic device of claim 50 wherein said first said another portion is in core logic of said programmable logic device.

53. (original) The programmable logic device of claim 50 wherein said second said another portion is a pin of said programmable logic device.

54. (original) The programmable logic device of claim 50 wherein said second said another portion is in core logic of said programmable logic device.

55. (previously presented) The programmable logic device of claim 49 wherein said digital signal processor has at least one of:

5 a second input programmably connectable to a first said another portion of said programmable logic device; and

a second output programmably connectable to a second said another portion of said programmable logic device.

56. (original) The programmable logic device of claim 55 wherein said first said another portion is a pin of said programmable logic device.

57. (original) The programmable logic device of claim 55 wherein said first said another portion is in core logic of said programmable logic device.

58. (original) The programmable logic device of claim 55 wherein said second said another portion is a pin of said programmable logic device.

59. (original) The programmable logic device of claim 55 wherein said second said another portion is in core logic of said programmable logic device.

60. (previously presented) The programmable logic device of claim 49 wherein said digital-to-analog converter has at least one of:

a second input programmably connectable to a
5 first said another portion of said programmable logic device;
and

a second output programmably connectable to a
second said another portion of said programmable logic
device.

61. (original) The programmable logic device of
claim 60 wherein said first said another portion is a pin of
said programmable logic device.

62. (original) The programmable logic device of
claim 60 wherein said first said another portion is in core
logic of said programmable logic device.

63. (original) The programmable logic device of
claim 60 wherein said second said another portion is a pin of
said programmable logic device.

64. (original) The programmable logic device of
claim 60 wherein said second said another portion is in core
logic of said programmable logic device.

65. (original) The programmable logic device of
claim 49 wherein said analog front end circuit comprises a
charge pump.

66. (previously presented) The programmable
logic device of claim 46 wherein said at least one component
comprises:

a phase-frequency detector having as inputs
5 said reference frequency and said output frequency, said
phase-frequency detector outputting digital comparison
signals indicating a relationship between said reference
frequency and said output frequency;

a digital counter circuit having said digital
10 comparison signals as inputs and outputting digital count
signals indicative of said comparison;

a digital signal processor having said digital count signals as inputs and outputting a digital control signal; and

15 a digital-to-analog converter having said digital control signal as an input and outputting an analog control signal that is input to said oscillator.

67. (previously presented) The programmable logic device of claim 66 wherein said digital signal processor has at least one of:

an additional input programmably connectable
5 to a first said another portion of said programmable logic device; and

a second output programmably connectable to a second said another portion of said programmable logic device.

68. (original) The programmable logic device of claim 67 wherein said first said another portion is a pin of said programmable logic device.

69. (original) The programmable logic device of claim 67 wherein said first said another portion is in core logic of said programmable logic device.

70. (original) The programmable logic device of claim 67 wherein said second said another portion is a pin of said programmable logic device.

71. (original) The programmable logic device of claim 67 wherein said second said another portion is in core logic of said programmable logic device.

72. (previously presented) The programmable logic device of claim 66 wherein said digital-to-analog converter has at least one of:

a second input programmably connectable to a
5 first said another portion of said programmable logic device;
and

a second output programmably connectable to a second said another portion of said programmable logic device.

73. (original) The programmable logic device of claim 72 wherein said first said another portion is a pin of said programmable logic device.

74. (original) The programmable logic device of claim 72 wherein said first said another portion is in core logic of said programmable logic device.

75. (original) The programmable logic device of claim 72 wherein said second said another portion is a pin of said programmable logic device.

76. (original) The programmable logic device of claim 72 wherein said second said another portion is in core logic of said programmable logic device.

77. (original) The programmable logic device of claim 46 wherein said oscillator is a voltage-controlled oscillator.

78. (original) The programmable logic device of claim 46 further comprising an output scaling counter downstream of said output terminal.

79. (original) The programmable logic device of claim 46 further comprising an input scaling counter upstream of said input terminal.

80. (original) The programmable logic device of claim 46 further comprising a feedback scaling counter between said output terminal and said feedback path.

81. (original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry;

a programmable logic device as defined in claim 46 coupled to the processing circuitry and the memory.

82. (original) A printed circuit board on which is mounted a programmable logic device as defined in claim 46.

83. (original) The printed circuit board defined in claim 82 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

84. (original) The printed circuit board defined in claim 83 further comprising:
processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.